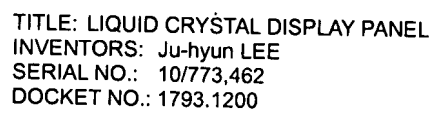
[illegible]



The circuit diagram shows a central processing unit 42 connected to various peripheral components. At the top, a rectangular block 44 is connected to three input lines entering the top of unit 42. These lines pass through a dashed box containing three inverters labeled 44a. A label 49 points to the first inverter. The output of this stage goes to a horizontal bus line 44b at the bottom. This bus line passes through another dashed box containing three transistors labeled T1. To the left of unit 42, a vertical block 46 is connected to three input lines entering the left side of unit 42. These lines pass through a dashed box containing three buffers or drivers labeled 46a. A label GL points to the first buffer, and DL points to the second. The output of this stage goes to a horizontal bus line 48. This bus line passes through a dashed box containing four memory elements or registers labeled 48a, 48b, 48c, and 48d. A label 48 points to the top register. Inside unit 42, there are several internal components: a diagonal hatched area 42c, a circle with a dot 42b, and a transistor T2. Various other labels like 42a and 46b point to specific internal nodes or components.